Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 7 are presently pending in the application. Claims 2 and 5 have been amended.

In item 1 of the above-identified Office Action, formal drawings were required. Formal drawings have been included herewith. More particularly, three (3) substitute sheets of drawings have been provided that replace the three drawing sheets originally filed in the instant application. Additionally, FIGS. 3 and 4 were amended to fill-in some vertical lines that did not come out on the copies filed. Two redlined sheets are additionally provided showing the corrections made to FIGS. 3 and 4.

In item 2 of the above-identified Office Action, Acknowledgement was made of Applicants' claim for foreign priority based on applications filed in Germany on September 30, 1998 and a PCT filed on September 17, 1999. However, it was noted in the Office Action that Applicant has not filed certified copies of the 198 45 002.8 and PCT/DE99/02992 applications, as required by 35 U.S.C. § 119(b). Applicants will file the certified copy of the German application, which is all that is required.

In item 3 of the Office Action, claim 5 was objected to as lacking the proper antecedent basis for the word "device" in that claim. The Examiner's recommended change has been made. Additionally, Claim 2 was objected to for an alleged lack of antecedent basis for the recitation of "the associated column numbers". Claim 2 has been amended to address the above concern.

In item 4 of the above-identified Office Action, claims 1 - 7 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,805,216 to Tabei et al ("**TABEI**") in view of U. S. Patent No. 5,471,478 to Mangan ("**MANGAN**").

Applicants respectfully traverse the above rejections.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

According to the presently claimed invention, a simple and advantageous method and device for correcting defective pixels of an image sensor is provided, wherein considerably less data have to be stored to address all the defect cells in the image sensor.

Claim 1 recites, among other limitations:

> "generating the defect signal from an image line address and an image column address such that **a pointer memory is addressed by the image line address, wherein the pointer memory contains a pointer for each of at least some of the image lines, the pointer addressing a defect column memory having stored therein column numbers of defective image columns;**" [emphasis added by Applicants]

Applicants' independent claim 5 additionally recites similar limitations, in connection with a defect memory unit including a pointer memory.

As such, Applicants' claimed invention relates to a "double indexed" addressing procedure, wherein a defect pointer memory is addressed to obtain a pointer, which points to a second defect memory (i.e., the defect column memory), in which the column address of a defect is stored.

Claim 1 further requires, among other limitations:

> "reading the column number from the defect column memory, comparing the column number with the column address, and forming therefrom the defect signal."

Claim 5 recites, among other limitations, a comparator to perform a function similar to that recited in claim 1. Thus, the "double indexed" addressing procedure of Applicants' claimed invention is used to generate a defect signal. Applicants' claimed invention reduces the amount of memory

required to store defect information, as both a line number **and** a column number are not needed to be stored for **each** defect. Rather, in Applicants' claimed invention, a pointer is obtained from the first memory, which is addressed by the line number, and then any number of column defects can be obtained from the second memory, using the same pointer (i.e., which identifies the defect's line number).

Neither the **TABEI** reference cited in the Office Action, nor the **MANGAN** reference, teach or suggest Applicants' claimed invention.

More particularly, none of the references cited in the Office Action teach or suggest Applicants' "double indexed" addressing procedure, wherein a first defect memory is addressed (i.e., by an image line number) to obtain a pointer to a second defect memory to obtain the column numbers where defects are present.

Rather, the **TABEI** reference discloses a defective pixel correction circuit like that of the prior art taught in the Background of the Invention section of the instant application. See **TABEI**, col. 7, lines 56 - 65; and col. 8, line 51. Thus, **TABEI** suffers from the disadvantage of the prior art taught in the Background of the instant invention

(i.e, that, for TV resolution, 404 kbits would be stored to identify defects).

The **TABEI** reference neither teaches, nor suggests, Applicants' claimed "double indexed" addressing procedure including a defect pointer memory, addressed by line number, and a second defect memory, addressed by a pointer from the defect pointer memory, to obtain the column numbers of defects associated with that line number. This deficiency of **TABEI** is noted in the Office Action on page 4, which states:

> "Tabei does not explicitly teach the defect memory device including a pointer memory, an address advancing device, and a defect column memory, whereby said pointer memory is addressed by the image line number and a content of address advancing device, said defect column memory, and said cell thus addressed addresses, via said address advancing device, said defect column memory, and said defect column memory outputs a defect column number for the line with the relevant image line number."

As such, Applicants' claims are believed to be patentable over the **TABEI** reference.

However, the Office Action, page 4, goes on to state:

> "Mangan teaches reading out data stored in a semiconductor memory (e.g., EEPROM) that includes a pointer memory, an address advancing device (for incrementing column/row), and a defect column memory whereby the pointer memory (for incrementing column/row), and a defect column memory whereby the pointer memory is addressed by row number and a content of a cell thus addressed addresses defect column memory

> via address advancing device. The defect column memory outputs a defect column number for the row with the relevant image line number (see Figs. 3, 4, 9A & 9B; col. 8, lines 39 - 65).
>
> Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Mangan with Tabei for reading out of the defective pixel locations from the defective memory by using line can column pointers as taught by Mangan to arrive at the Applicant's claimed invention so that accessing to the defective pixel positions is performed in a short time since the defective pixel positions have been pointed by loading row and column pointers in the memory map/table prior to taking image in."

Applicants respectfully disagree with the statement made in the Office Action, as to what is taught in, or would be obvious from, the **MANGAN** reference. More particularly, the **MANGAN** reference neither teaches, nor suggests, Applicants' particularly claimed "double indexed" addressing procedure, among other limitations of Applicants' claims.

Rather, the **MANGAN** reference relates to a flash EEPROM array data and header file structure. The **MANGAN** reference discloses a common, column redundancy and row redundancy principle, which is used in a storage memory for providing additional memory cells used to replace defective memory cells in a memory matrix. To accomplish this, **MANGAN** discloses having one or more "bad bit" pointers in each of the rows of the memory matrix. However, in contrast to Applicants' claimed invention, the bad bit pointers of **MANGAN** do not include a pointer to **a further memory** (i.e, Applicants'

claimed defect column memory), **in which the actual address of the defect column is stored**. According to **MANGAN**, the column number of the defective column is directly stored in the bad bit pointer. This is described in col. 8 of **MANGAN**, lines 4 - 16, which states:

> "If the data read from row 0 of the stack 215 is satisfactory, a next step 341 sets a compare function in the controller to include the pointer in the field 249 of row 0 of stack 215. A next step 343 then points to one or more bits in row 1 of the stack 215 which are to be read at the same time. In the example being described, data is transferred between the controller and the EEPROM chips a pair at a time. **A comparison indicated at a step 345 looks to see if the addresses of the bit pair include that of the bad bit pointer in field 249 (FIG. 6).** If not, the pair of bits is read, as indicated in a step 347. If, on the other hand, the addressed bits of row 1 include that of the field 249 pointer, a step 349 increments the bit address to the next bit pair in sequence along row 1." [emphasis added by Applicants]

As can be seen from the **MANGAN** reference, the content of the bad bit pointer in **MANGAN** **is** the column number of the defective cell, which, in to the system of **MANGAN**, completes the address of the defective cell. The bad bit pointer of **MANGAN does not point to a second memory containing the column address**, as is required by Applicants' claims, but, rather, in **MANGAN**, the bad bit pointer **is**, itself, the column address. See also **MANGAN**, col. 10, lines 13 - 17 ("If the data does not compare, a step 441 identifies the bad cell or cells by address which are responsible for the bad bits, **and then adds**

that address in the form of a bad bit pointer to the bad bit pointer fields 235-237 of the stack 215 in its proper order.")

Further, in **MANGAN**, the bad column pointer is the corresponding addressing procedure for the so-called row redundancy addressing, wherein the above addressing procedure for the bad bit pointers is similarly implemented with regard to bad column pointers. In other words, the bad column pointers directly include the row number of the defective cell, or, as disclosed in col. 8 of **MANGAN**, lines 48 - 53, a flag indicating that the entire column is defective. This differs from Applicants' claimed invention, wherein a pointer in the defect pointer memory **actually points to** a second memory which stores the defect column address.

As the bad bit pointer of **MANGAN** points directly to the defective cell (i.e, the pointer includes the number of the defective column), **MANGAN** neither teaches, nor suggests Applicants' claimed invention. More particularly, in addition to other limitations of Applicants' claimed invention, **MANGAN**, like **TABEI**, fails to teach or suggest Applicants' particularly claimed "double indexed" addressing procedure including a defect pointer memory, addressed by line number, and a second defect memory, addressed by a pointer from the defect pointer memory, to obtain the column numbers of defects.

Because neither of the cited references teach or suggest, among other limitations of Applicants' claims, Applicants' particularly claimed "double indexed" addressing procedure, it is believed that the present claims are patentable over the **TABEI** and **MANGAN** references, taken alone, or in combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In view of the foregoing, reconsideration and allowance of claims 1 - 7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Kerry P. Sisselman
Reg. No. 37,237

For Applicants

KPS:cgm

March 1, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Amendments to the Drawings:

Formal drawings have been included herewith. More particularly, three (3) substitute sheets of drawings have been provided that replace the three drawing sheets originally filed in the instant application.

Additionally, FIGS. 3 and 4 were amended to fill-in some vertical lines that did not come out on the copies filed. Two redlined sheets are provided showing the corrections made to FIGS. 3 and 4.

Attachment: Three (3) Replacement Sheets
Two (2) Annotated Sheets Showing Changes

FIG 3

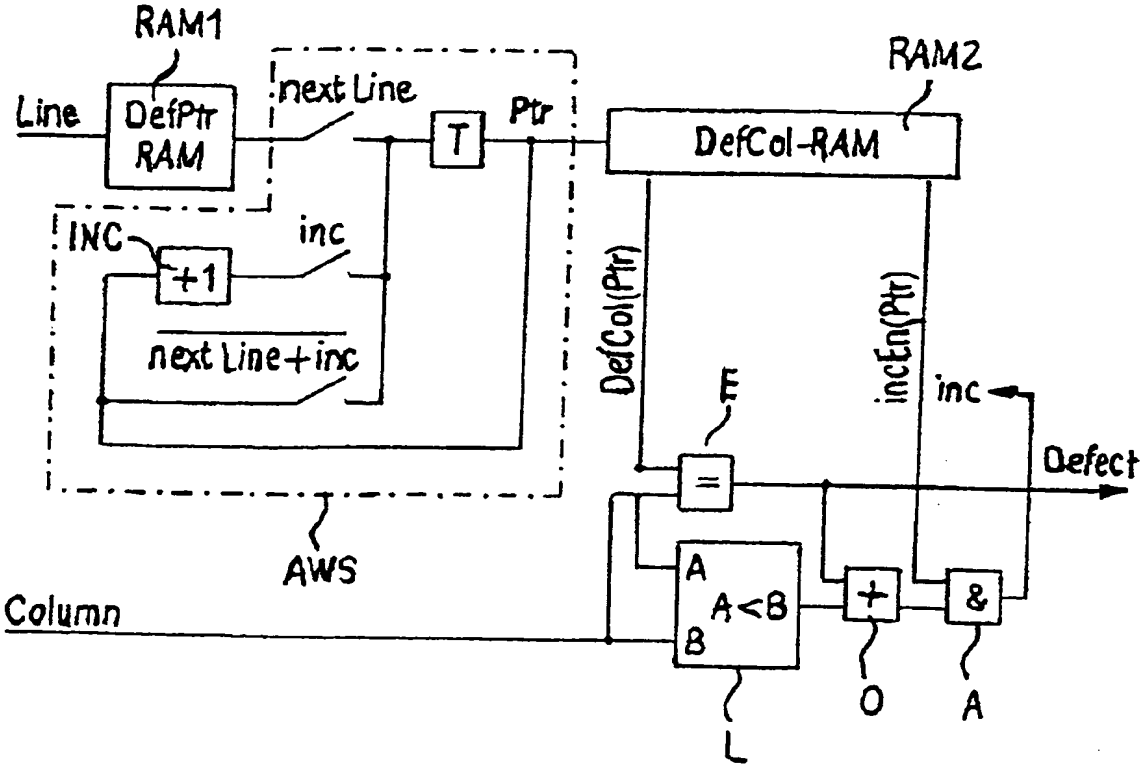

FIG 4